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06CS81

Eighth Semester B.E. Degree Examination, December 2010
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. List and explain four important technologies, which have led to the improvements in computer system. **(07 Marks)**

b. The given data presents the power consumption of several computer system components:

Component	Product	Performance	Power
Processor	Sun Niagara 8-core	1.2 GHz	72-79 W
DRAM	Kingston 1 GB	184 – pin	3.7 W
Hard drive	Diamond Max	7200 rpm	7.9 W read 4.0 W idle

i) Assuming the maximum load for each component, a power supply efficiency of 70%, what wattage must the server's power supply deliver to a system with a Sun Niagara 8-core chip, 2 GB 184-pin Kingston DRAM and 7200 rpm hard drives?

ii) How much power will the 7200 rpm disk drive consume, if it is idle roughly 40% of the time?

iii) Assume that for the same set of requests, a 5400 rpm disk will require twice as much time to read data as a 10800 rpm disk. What percentage of time would the 5400 rpm disk drive be idle to perform the same transaction as in part (ii)? **(07 Marks)**

c. We will run two applications on dual Pentium processor, but the resource requirements are not the same. The first application needs 80% of the resources, and the other only 20% of the resources.

i) Given that 40% of the first application is parallelizable, how much speed up will we achieve with that application, if run in isolation?

ii) Given that 99% of the second application is parallelizable, how much speed up will this application observe, if run in isolation?

iii) Given that 40% of the first application is parallelizable, how much overall system speedup would you observe, if we parallelized it? **(06 Marks)**

2 a. List pipeline hazards. Explain any one in detail. **(07 Marks)**

b. List and explain five different ways of classifying exception in a computer system. **(07 Marks)**

c. An unpipelined machine has 10 ns clock cycle and it uses four cycles for ALU operations and branches, five cycles for memory operations. Assume that relative frequencies of these operations are 40%, 20% and 40% respectively. Suppose due to clock skew and set up, pipelining the machine adds 1 ns overhead to the clock. Find the speed up from pipelining. **(06 Marks)**

3 a. Show how the below loop would look on MIPS 5-stage pipeline, under the following situations. Find the number of cycles per iteration, for each case. Assume the latencies for integer and floating point operations, as given in the prescribed text book.

```
Loop :  L . D      F0, 0(R1)
        ADD . D    F4, F0, F2
        S . D      F4, 0(R1)
        DADDUI     R1, R1, # - 8
        BNE        R1, R2, loop
```

Question No.3(a) continued...

i) Without scheduling and without loop unrolling.
ii) With scheduling and without loop unrolling.
iii) With loop unrolling four times and without scheduling.
iv) With loop unrolling four times and with scheduling. **(12 Marks)**

b. What is the drawback of 1-bit dynamic branch prediction method? Clearly state, how it is overcome in 2-bit prediction. Give the state transition diagram of 2-bit predictor. **(08 Marks)**

4 a. Explain the salient features of VLIW processor. **(08 Marks)**
b. Explain branch-target buffer. **(08 Marks)**
c. Write a short note on value predictors. **(04 Marks)**

PART – B

5 a. What is multiprocessor cache coherence? List two approaches to cache coherence protocol. Give the state diagram for write-invalidate write-back cache coherence protocol. Explain the three states of a block. **(12 Marks)**
b. List and explain any three hardware primitives to implement synchronization. **(08 Marks)**

6 a. Assume we have a computer where CPI is 1.0 when all memory accesses hit in the cache. The only data accesses are loads and stores, and these total 50% of the instructions. If the miss penalty is 25 cycles and miss rate is 2%, how much faster would the computer be, if all instructions were cache hits? **(08 Marks)**
b. Briefly explain four basic cache optimization methods. **(12 Marks)**

7 a. List and explain three C's model that sorts all cache misses. **(06 Marks)**
b. Explain the optimization methods mentioned below :
i) Trace cache to reduce hit time
ii) Non-blocking cache to increase cache bandwidth
iii) Multi banked cache to increase cache bandwidth. **(09 Marks)**
c. Briefly explain how memory protection is enforced via virtual memory. **(05 Marks)**

8 a. Consider the loop below:

```
for (i = 1 ; i ≤ 100 ; i = i + 1) {
    A [ i ] = A [ i ] + B [ i ] ; 1 * S1 * 1
    B [ i + 1 ] = C [ i ] + D [ i ] ; 1 * S2 * 1
}
```

What are the dependences between S1 and S2? Is this loop parallel? If not, show how to make it parallel. **(08 Marks)**
b. Explain Intel IA-64 architecture. **(12 Marks)**

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06CS82

Eighth Semester B.E. Degree Examination, December 2010
System Modeling and Simulation

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, choosing atleast TWO questions from each part.***

PART – A

1 a. When is a simulation an appropriate tool? When is it not? **(12 Marks)**
b. Explain the various components of simulation with an example. **(08 Marks)**

2 a. Explain the model of 'single channel queue' in detail. **(12 Marks)**
b. What is list processing? Explain the basic operations of list processing. **(08 Marks)**

3 a. Briefly explain the various probability terminologies and concepts. **(12 Marks)**
b. What is Poisson process? Mention the properties of Poisson process. **(08 Marks)**

4 a. Explain the various steady state parameters of M/G/1 queue. **(08 Marks)**
b. Explain the service times and server mechanics used in queuing system with an example. **(08 Marks)**
c. What is networks of queue? Mention the general assumptions for a stable system with infinite calling population. **(04 Marks)**

PART – B

5 a. Briefly explain the various techniques used to generate random numbers. **(12 Marks)**
b. Explain any two inverse transform techniques. **(08 Marks)**

6 a. Mention the important points to be noted while collecting data. **(08 Marks)**
b. Briefly explain the suggested estimators for distributions often used in simulation. **(12 Marks)**

7 a. Briefly explain the confidence – interval estimation method. **(10 Marks)**
b. Explain the two methods to specify the initial conditions in steady state simulation. **(10 Marks)**

8 a. Differentiate the processes of verification and validation. **(04 Marks)**
b. Explain the 3 steps involved in model building. **(06 Marks)**
c. Explain the iterative process of calibrating a model. **(10 Marks)**

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06CS834
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Eighth Semester B.E. Degree Examination, December 2010
Network Management Systems

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Define network management. Explain network management, goals and functions, with necessary function grouping figure. **(12 Marks)**

b. What are the challenges of information technology managers in managing the network? **(08 Marks)**

2 a. Explain the different network management standards. **(08 Marks)**

b. What is basic encoding rule? Explain. Using basic encoding rule, encode the data defined as OCTETSTRING (UNIVERSAL 4) of a value "OCIB" H. **(06 Marks)**

c. Explain organization model, with a neat diagram. **(06 Marks)**

3 a. Explain the classification of SNMP ASN.1 data types, with a neat diagram. **(06 Marks)**

b. Explain SNMP network management architecture, with a neat diagram. **(10 Marks)**

c. With a neat sketch, explain proxy server organizational model. **(04 Marks)**

4 a. How are the managed objects defined in network management? Explain. **(10 Marks)**

b. Define and explain SNMP access policies in SNMP management. **(10 Marks)**

PART – B

5 a. With a neat diagram, explain the RMONI group and functions. **(10 Marks)**

b. Explain the RMON MIB frame work and ATM probe location, with a neat diagram. **(10 Marks)**

6 a. What is ATM LAN emulation? Explain ATM LAN emulation network by using layered architecture. **(08 Marks)**

b. Discuss the generic troubles in ATM network elements. **(05 Marks)**

c. Explain the ATM network reference model. **(07 Marks)**

7 a. Explain the complete AOSL system reference model. **(10 Marks)**

b. Explain the rule based reasoning and model based reasoning correlation techniques used to isolate and localize faults in network. **(10 Marks)**

8 Write short notes on the following: **(20 Marks)**

a. Security management

b. Performance management

c. HFC technology

d. Broadband access technology.

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Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

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06CS846

Eighth Semester B.E. Degree Examination, December 2010
Programming Languages

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain how programming languages are classified? **(06 Marks)**

b. Explain the difference between interpretation and compilation. What are the advantages and disadvantages of two approaches? **(06 Marks)**

c. Explain the three principal storage allocation mechanisms, with respect to the object lifetime. **(08 Marks)**

2 a. What is deep and shallow binding? Explain briefly. **(06 Marks)**

b. List and explain the major categories of control flow mechanism. **(10 Marks)**

c. What is short circuit evaluation? Explain with example. **(04 Marks)**

3 a. What are the structured alternatives to goto statements? **(08 Marks)**

b. What is tail recursive function? Why is tail recursion important? **(06 Marks)**

c. What is lazy evaluation? Explain promises and memorization? **(06 Marks)**

4 a. What is the difference between type equivalence and type compatibility? **(10 Marks)**

b. For the following three dimensional array (contiguous layout) calculate the address of A [i, j, k] :
A : array $[L_1 \ldots U_1]$ of array $[L_2 \ldots U_2]$ of array $[L_3 \ldots U_3]$ of element type. Write the instruction sequence to load A [i, j, k] into a register. **(10 Marks)**

PART – B

5 a. Represent the following tree in ML and LISP :

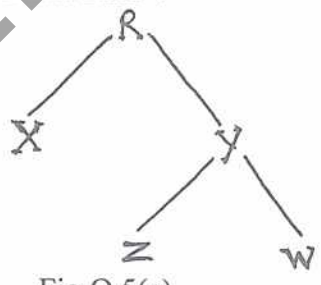

Fig.Q.5(a). **(08 Marks)**

b. Explain the basic list operations in LISP. **(06 Marks)**

c. What are dangling references? How are they created? What are the problems? **(06 Marks)**

6 a. Explain the operation of typical calling sequence. **(08 Marks)**

b. What is call – by – sharing? How is it different from call – by – value and call – by – reference? **(06 Marks)**

c. Explain the exception handler of functional language ML, with example. **(06 Marks)**

7 a. What is cactus stack? Explain its structures and use. **(10 Marks)**

b. Explain the difference between dynamic and static method binding, with example. **(10 Marks)**

8 a. What are the features of functional programming languages? **(06 Marks)**

b. What is unification? List the unification rules for prolog. **(06 Marks)**

c. What are the common characteristics of scripting language? **(08 Marks)**

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